(Model Paper) **C –23, EC -405**

State Board of Technical Education and Training, A. P

Diploma in Electronics and Communication Engineering (DECE)

IV Semester

Subject Name: DIGITAL LOGIC DESIGN USING VERILOG HDL

Sub Code: EC - 405

Time: 90 minutes **Unit Test I** **Max.Marks:40**

Part-A **16Marks**

Instructions: (1) Answer **all** questions.
(2) First question carries **four** marks, each question of remaining carries **three** marks

1. Fill the following blanks with one word
   a) HDL stands for_____ (CO 1)
   b) VLSI stands for_____ (CO 1)
   c) Write any one assignment statements in data flow modelling_____ (CO 2)
   d) Write any two types of timing controls used in Verilog HDL_____ (CO 3)
2. Compare VHDL and Verilog HDL (CO1)
3. Define expression and operator. (CO 1)
4. List the advantages of data flow modelling over gate level modelling (CO 2)
5. Differentiate between case, caseX branching statements (CO 3)

Part-B **3×8=24**

Instructions: (1) Answer **all** questions.
(2) Each question carries **eight** marks
(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

6. (a) Explain the steps involved in the design flow for the VLSI IC design (CO1)
   or
   (b) Explain different data types like value set, nets, registers, vectors, integer, real and time Register data types (CO1)
7. (a) Explain Rise, fall and turn-off delays in the gate level modelling (CO2)
   or
   (b)Explain different types of delays used in the data flow level modelling (CO2)
8. (a) Explain structural procedures - initial and always statements (CO3)
   or
   (b) Explain conditional statements used in Verilog HDL (CO3)

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Subject Name: DIGITAL LOGIC DESIGN USING VERILOG HDL

Sub Code: **EC - 405**

Time: 90 minutes **Unit Test II** Max.Marks:40

Part-A **16Marks**

Instructions: (1) Answer **all** questions.
(2) First question carries **four** marks, each question of remaining carries **three** marks

1. Fill the following blanks with one word

   a) Write any one difference between conditional if statement and case statements (CO3)

   b) Write any one example for combinational logic circuit (CO4)

   c) Write any one example for sequential logic circuit (CO4)

   d) PLA stands for _____ (CO5)

2. List the types of UDPs (CO3)
3. Compare RTL level and structural level modelling (CO4)
4. List various design tools which are useful in different stages of design (CO5)
5. List any 3 applications of programmable logic devices. (CO5)

Part-B **3×8=24**

Instructions: (1) Answer **all** questions.
(2) Each question carries **eight** marks
(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

6. (a) Explain looping statements such as while, for, repeat, and forever. (CO 3)

   or

   (b)Explain combinational UDPs with example (CO 3)

7. (a) Design a divide by 3 counters (CO4)

   or

   (b) Explain the structure of stimulus module (CO4)

8. (a) Explain the architecture of CPLD (CO5)

   or

   (b) Explain the architecture of PLAs. (CO5)

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MODEL PAPER
BOARD DIPLOMA EXAMINATIONS
IV SEMESTER
Sub Code: EC – 405
Subject Name: DIGITAL LOGIC DESIGN USING VERILOG HDL
SEMESTER END EXAMINATION

TIME: 3 HOURS MAX MARKS:80

Part-A **10×3=30**

Instructions: (1) Answer **all** questions.
(2) Each question carries **three** marks
(3) Answer should be brief and straight to the point and shall not exceed five simple sentences.

1. Compare VHDL and Verilog HDL (CO1)
2. Define expression and operator (CO1)
3. List the advantages of data flow modelling over gate level modelling (CO2)
4. List different types of delays used in the data flow level modelling (CO2)
5. Differentiate between case, caseX branching statement (CO3)
6. List the types of UDPs (CO3)
7. Compare RTL level and structural level modelling (CO4)
8. Differentiate between Asynchronous and Synchronous Clock (CO4)
9. List various design tools which are useful in different stages of design (CO5)
10. List any 3 applications of programmable logic devices. (CO5)

Part-B **5×10=50**

Instructions: (1) Answer **any Five** questions.
(2) Each question carries **TEN** marks
(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Explain the steps involved in the design flow for the VLSI IC design (CO1)
12. Explain different data types like value set, nets, registers, vectors, integer, real and time Register data types (CO1)
13. Explain Rise, fall and turn-off delays in the gate level modelling (CO1)
14. Explain looping statements such as while, for, repeat, and forever. (CO3)
15. Explain combinational UDPs with example (CO3)
16. Design a divide by 3 counter (CO4)
17. Explain the structure of stimulus module (CO4)
18. Explain the architecture of CPLD (CO5)

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