R20

II B. Tech I Semester Supplementary Examinations, July - 2023
SWITCHINNG THEORY AND LOGIC DESIGN
(Com to ECE, EIE, ECT)

Time: 3 hours   Max. Marks: 70

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1   a)   The solution to the quadratic equation $x^2-11x+22=0$ is x=3 and x=6. What is the base of number?   [5M]

    b)   Convert the following to decimal and then to octal.   [6M]
         (i)4204_{16}
         (ii)1010011_2

    c)   Perform the following using BCD arithmetic $(79)_{10} + (177)_{10}$ [3M]

Or

2   a)   Obtain the simplified POS and SOP expression for the function using k-maps: [8M]
         $F(A,B,C,D)=\Sigma(1,3,5,8,9,13)+\Sigma\ d(0,7,12,14)$

    b)   Obtain the dual of the following Boolean expressions   [6M]
         (i) AB+A(B+C)+B'(B+D)   (ii)A+B+A'B'C
UNIT-II

3   a)   Simplify the following function using k-maps and implement the same using NAND gates.   [7M]
         $F(A,B,C)=\Sigma(0,2,4,5,6,7)$

    b)   Briefly explain the tabulation procedure for the determination of prime implicants.   [7M]

Or

4   a)   Draw and explain the operation of 4-bit binary adder-subtractor circuit.   [4M]

    b)   Design a combinational circuit that converts a 4-bit binary number to 4-bit gray code number. Implement the circuit with Exclusive-OR gates.   [10M]
UNIT-III

5   a)   Realize full adder and full subtractor using 8:1 MUX.   [8M]

    b)   Design a 3-bit priority encoder with one example.   [6M]

Or

6   a)   Realize the following four boolean functions using PAL.   [10M]
         $F_1(w,x,y,z) = \sum m(0,1,2,3,7,9,11)$
         $F_2(w,x,y,z) = \sum m(0,1,2,3,10,12,14)$
         $F_3(w,x,y,z) = \sum m(0,1,2,3,10,13,15)$
         $F_4(w,x,y,z) = \sum m(4,5,6,7,9,15)$

    b)   Draw and explain the basic structure of PROM.   [4M]

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UNIT-IV

7 a) Draw the logic diagram of parallel-in, serial-out shift register and explain its operation.   [6M]

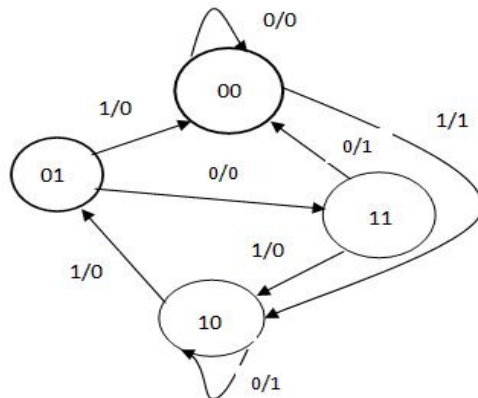   b) Convert a D flip-flop to T flip-flop with an example.   [8M]

Or

8 a) Explain about Ring counter.   [7M]

   b) Explain the operation of the bi-directional shift register.   [7M]

UNIT-V

9 a) Design an FSM for serial sequence detector with the pattern "1010" with overlapping and with non-over lapping.   [10M]

   b) Give the comparison between Mealy and Moore models.   [4M]

Or

10 a) A sequential circuit has one input and one output. The state diagram is shown below: [10M]

      Design the sequential circuit with JK flip-flop

    b) Write a brief note on Finite State Machines.   [4M]