Code No:R2022421 **R20** **SET - 1**

II B. Tech II Semester Supplementary Examinations, December - 2023
COMPUTER ORGANIZATION
(Common to CSE(AIML),CSE(AI),CSE(DS),CSE(AIDS),AIDS &AIML,CSD)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1 a) What is an overflow condition in number arithmetic? How is it detected? Perform the arithmetic operations (+70) + (+80) and (-70) + (-80) withbinary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is asign reversal. [8M]

b) Derive an algorithm in flowchart form for adding and subtracting two fixed-point binary numbers when negative numbers are in signed-1's complement representation. [6M]

Or

2 a) Briefly explain the historical perspective of computer generations. [7M]

b) Show the step-by-step multiplication process using Booth's algorithm when the following binary numbers(+ 15) and (+13) are multiplied. Assume 5-bit registers that hold signed numbers. The multiplicand is + 15. [7M]

UNIT-II

3 a) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right,followed by a logical shift-right and a circular shift-left. [7M]

b) Discuss in detail any seven memory-referencing instructions and also write the functions of each. [7M]

Or

4 a) What do you mean by three-state logic? Explain the construction of a bus system with three-state buffers with a block diagram. [7M]

b) A computer uses a memory of 65,536 words with eight bits in each word.It has the following registers: PC, AR, T R (16 bits each), and AC, DR, IR(eight bits each). A memory-reference instruction consists of three words: an 8-bit operation-code (one word) and a 16-bit address (in the next two words).All operands are eight bits. There is no indirect bit. [7M]

(i) Draw a block diagram of the computer showing the memory and registers. (Do not use a common bus).

(ii) List the sequence of microoperations for fetching a memory reference instruction and then placing the operand in DR. Start from timing signal T_o.

UNIT-III

5 a) Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result. [7M]
(3 + 4)[10(2 + 6) + 8]

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b) Describe the micro instruction format for the control memory. [7M]

Or

6 a) What are the basic differences between a branch instruction, a call subroutine instruction and program interrupt? Explain with an example. [7M]

b) Define the following: [7M]
(i) micro-operation
(ii) microinstruction
(iii) microprogram
(iv) microcode.

UNIT-IV

7 a) Explain the hardware organization of associative memory. [7M]

b) Why are the read and write control lines in a DMA controller bidirectional?Under what condition and for what purpose are they used as inputs? Underwhat condition and for what purpose are they used as outputs. [7M]

Or

8 a) Write short notes on [7M]
(i) Magnetic disks
(ii) Magnetic tapes

b) Describe the daisy-chaining method of establishing priority of interrupts. [7M]

UNIT-V

9 a) Draw a diagram showing the structure of a four-dimensional hypercubenetwork. Use all the paths available from node 7 to node 9 that use the minimum number of intermediate nodes. [7M]

b) What do you mean by data dependency conflicts in instruction pipelining? Discuss any two methods that the pipelined computers use to deal with such conflicts. [7M]

Or

10 a) Discuss in detail about RISC pipeline. [7M]

b) Explain delayed branch technique with a simple example. [7M]