Code No: R2022022 **R20** **SET - 1**

II B. Tech II Semester Supplementary Examinations, December - 2023

DIGITAL ELECTRONICS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~~

UNIT-I

1 a) Convert each of the following decimal numbers to excess-3 code. [7M]
i) $(18)_{10}$ ii) $(56)_{10}$

b) What is Hamming code? How is the Hamming code word tested and corrected? [7M]

OR

2 Draw the symbols and Write the Boolean expressions and truth tables of following logic gates: [14M]
i) NOT ii) AND iii) EX-OR iv) EX-NOR v) NAND vi) OR

UNIT-II

3 a) Compare between combinational and sequential circuits. [7M]

b) Construct a full adder using only two half adders and one OR gate. [7M]

OR

4 a) Minimize the following expression using K-map and realize using NAND Gates. [7M]
$F(A,B,C,D) = \sum m(0,1,2,9,11) + d(8,10,14,15)$.

b) Simplify the function using K - map method [7M]
$F(A,B,C,D) = \sum(4,5,7,12,14,15) + \sum d(3,8,10)$.

UNIT-III

5 a) Implement the following Boolean function with PLA $F(A,B,C) = \sum m(0,1,2,4)$. [7M]

b) Explain the operation of 3 to 8 line decoder with the help of a truth table. [7M]

OR

6 a) Explain the design procedure 3 to 8 decoder with suitable logic diagram. [7M]

b) Draw and explain the logic diagram of a 4-to-1 line multiplexer with logic gates. [7M]

UNIT-IV

7 Explain the operation of following flip flops using its block diagrams and truth tables. What are their limitations? [14M]
a) RS flip flop b) JK flip flop

OR

8 a) Obtain the characteristic equations of D and T flip flops. [7M]

b) Draw the circuit diagram of a 4-bit binary counter with parallel load and explain itsworking with its function table. [7M]

UNIT-V

9 a) What is hazard? How are static hazards eliminated? [7M]

b) With a neat block diagram, explain the moore model of a clocked synchronous sequential circuit. [7M]

OR

10 a) Illustrate partition techniques in sequential circuits. [7M]

b) Explain the procedure for state minimization using merger graph and merger table. [7M]

|'''|'|'|''||'''||||
~~~~~~~~~~~~~~~~~~~~~~~~~