Code No:R2022042 **R20** **SET - 1**

II B. Tech II Semester Supplementary Examinations, December - 2023

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1	a)	Discuss (i) Block Statement (ii) Generics in VHDL	[4M]
	b)	Explain the various data objects supported by VHDL. Give the necessary examples.	[10M]

Or

2	a)	Discuss in detail about different levels of abstraction in VHDL.	[7M]
	b)	Explain the use of packages. Give the syntax and structure of a package in VHDL.	[7M]

UNIT-II

3	a)	Design gray to binary code converter and write its VHDL code.	[7M]
	b)	Design priority encoder and write its VHDL code.	[7M]

Or

4	a)	Design a parity generator and write its VHDL code.	[7M]
	b)	Design a single bit comparator and write its VHDL code.	[7M]

UNIT-III

5	a)	Design a 4 bit asynchronous counter and write its VHDL code.	[7M]
	b)	Design a shift right register using IC and explain its operation.	[7M]

Or

6	a)	Design an universal shift register using IC and explain its operation.	[7M]
	b)	Design a 4 bit LFSR with an initial state as 6.	[7M]

UNIT-IV

7	a)	Design NAND gate using (i) pseudo nmos (ii) depletion load nmos (iii) CMOS	[9M]
	b)	Design a 2 input OR gate using a pass transistor logic.	[5M]

Or

8	a)	Design AOI and OAI using CMOS.	[7M]
	b)	Design the following function using CMOS:Y=A(B+C)'	[7M]

UNIT-V

9	a)	Design and discuss master-slave flip-flop using CMOS.	[7M]
	b)	Discuss the behavior bistable element using inverters.	[7M]

Or

10	a)	Design and discuss basic SR latch using CMOS gate.	[7M]
	b)	Design D flip flop using CMOS and transmission gates.	[7M]

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