Code No:R2022042 **R20** **SET - 1**

II B. Tech II Semester Regular/Supplementary Examinations, July- 2023

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1	a)	Write different modeling styles in VHDL with suitable examples.	[7M]
	b)	Define the following terms relevant to Verilog HDL. i) Simulation versus synthesis ii) PLI iii) System Tasks.	[7M]

Or

2	a)	Explain the four main data types in VHDL.	[7M]
	b)	What are different operators in VHDL?	[7M]

UNIT-II

3	a)	What are the differences between encoder and multiplexer and design a 2 to 4 multiplexer using74X157 and write a VHDL code for it.	[7M]
	b)	Design a 5 to 32 decoder using 74X138S write its VHDL code.	[7M]

Or

4	a)	Design a full adder considering half adder as a component.	[7M]
	b)	Write a VHDL code for a 8-bit tri state inverter using 74X541 IC.	[7M]

UNIT-III

5	a)	Explain the operation of 8-bit register with the help of 74X374 IC.	[7M]
	b)	Write a VHDL behavioral model of a 16 bit registers.	[7M]

Or

6		Design, implement and explain a 4 bit binary counter using 74X 163 IC and write its VHDL code.	[14M]

UNIT-IV

7	a)	Design a half adder using CMOS.	[7M]
	b)	Develop an SOP function $F = \overline{A + BC}$ using CMOS.	[7M]

Or

8	a)	What are the demerits of a CMOS gate? Discuss.	[7M]
	b)	Develop a 2 input OR- gate using pseudo NMOS.	[7M]

UNIT-V

9	a)	Design a T flip flop using CMOS.	[7M]
	b)	Develop a complementary pass transistor logics.	[7M]

Or

10	a)	Design and explain NOR based SR latch using CMOS.	[7M]
	b)	Design D latch using CMOS inverters and a transmission gate as switches.	[7M]
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Code No:R2022042 **R20** **SET - 2**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1	a)	Write about (i) signal assignments (ii) variable assignments (iii) component declaration (iv) component instantiation with suitable examples.	[7M]
	b)	Mention data types used in Verilog HDL.	[7M]

Or

2	a)	Write the syntax of a case statement with a suitable example.	[7M]
	b)	Explain the use of packages. Give the syntax and structure as a package in VHDL?	[7M]

UNIT-II

3	a)	Design a binary to gray code converter and write VHDL code for it.	[7M]
	b)	Develop a 4 bit ALU and write its VHDL code.	[7M]

Or

4	a)	Design a 8-bit priority encoder using 74X148 IC and write its VHDL code.	[7M]
	b)	Starting from a single bit full adder as a component, write down the structural VHDL description for a 4-bit parallel adder?	[7M]

UNIT-III

5	a)	Design and develop a modulo 8 binary counter and decoder using 74X163 and 74X 138.	[7M]
	b)	Explain 74X169 up/down counter and write its VHDL code.	[7M]

Or

6	a)	Discuss the logic circuit of 74 X #77 register. Write a VHDL program for the same in structural style.	[7M]
	b)	Design synchronous serial counter using 74 X 163 and write its VHDL code.	[7M]

UNIT-IV

7	a)	Design an SOP function $F = \overline{AB + CD}$ with CMOS logic.	[7M]
	b)	Design an AOI LOGIC with CMOS logic.	[7M]

Or

8		Design the following functions using CMOS logic (i) f=[(ab)+ (cd)]' (ii) f=a(b+c)	[14M]

UNIT-V

9	a)	What are the disadvantages of a pass transistor? Explain clearly.	[7M]
	b)	Develop a 2 input AND gate using pass transistor.	[7M]

Or

10	a)	What is a bistable element? Design bistable device with the help of CMOS inverters and also discuss transient analysis.	[10M]
	b)	Design schimth trigger using CMOS and explain.	[4M]

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Code No:R2022042 **R20** **SET - 3**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1	a)	Write the syntax with a suitable example of (i) loop (ii) if (iii) libraries	[7M]
	b)	Define strengths and content resolution in VERILOG.	[7M]

Or

2	a)	Write about 6 different concurrent statements in VHDL.	[7M]
	b)	What are different data objects in VHDL and explain.	[7M]

UNIT-II

3	a)	Write a VHDL code to implement half and full adder using Data flow style.	[7M]
	b)	Design a 74X280 9 bit odd/even parity generator and write its VHDL code.	[7M]

Or

4		Write a VHDL code to implement 2*2 unsigned combinational Array Multiplier.	[14M]

UNIT-III

5		What are the four functional states of universal shift register using 74X194 explain its modes and write its VHDL code.	[14M]

Or

6	a)	Discuss a self correcting 4 bit 4 state ring counter with a single circulating 1 the help of 74X 194	[7M]
	b)	Discuss the concept of LFSR with the help of a circuit using IC .	[7M]

UNIT-IV

7	a)	Discuss NMOS gate with different loads.	[7M]
	b)	Can you design 3 input NAND gate using CMOS logic?	[7M]

Or

8	a)	Design a CMOS full adder.	[7M]
	b)	Develop an AND operation using pass transistor logic.	[7M]

UNIT-V

9	a)	Design Master slave D flip flop using transmission gates.	[7M]
	b)	Design NOR based SR Latch using CMOS logic.	[7M]

Or

10	a)	Design NAND based SR Latch using CMOS logic.	[7M]
	b)	Design D latch using transmission gates and explain the operation.	[7M]

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Code No:R2022042 **R20** **SET - 4**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1	a)	What is NEXT, EXIT, ASSERTION, NULL statements with suitable example	[7M]
	b)	Explain with examples about: i) Display tasks ii) Strobe tasks iii) Monitor tasks in VERILOG	[7M]
		Or	
2	a)	Write about block statement, process statement, selected signal assignment statement with examples.	[7M]
	b)	Explain assignments with delays in VERILOG.	[7M]

UNIT-II

3	a)	Design a 74X 85 4 bit comparator and write its VHDL code.	[7M]
	b)	Convert gray to binary and write its VHDL code for it.	[7M]
		Or	
4		What are the advantages of a carry look ahead adder, design and write a VHDL code for it.	[14M]

UNIT-III

5	a)	Discuss a 4 bit 8 state ring counter with the help of 74X 194.	[7M]
	b)	Explain the basic principle behind LFSR and draw its structure.	[7M]
		Or	
6	a)	Discuss a 4 bit 8 state johnson counter with a single circulating 1 the help of 74X 194.	[7M]
	b)	Write a VHDL code for 8 bit shift register.	[7M]

UNIT-IV

7	a)	Implement the following functions using NMOS (i) F= A (B+C) (ii) F=AB+CD.	[7M]
	b)	Develop an AND operation using pass transistor logic.	[7M]
		Or	
8	a)	Design 2X1 mux using a pass transistor logic.	[7M]
	b)	Develop AOI logic using CMOS devices.	[7M]

UNIT-V

9		Design (i) D latch (ii) SR latch using CMOS.	[14M]
		Or	
10		Design a master slave flip flop with CMOS.	[14M]

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