Code No: R2032042 **R20** SET -1

III B. Tech II Semester Regular Examinations, July -2023
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) With a neat sketch explain BICMOS fabrication in p-well process and also explain its operation. [7M]
   b) Write down the equations for Ids of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region. [7M]

(OR)

2. a) Explain the PMOS enhancement mode fabrication process for different conditions of Vds? [7M]
   b) An NMOS transistor is operating in active region with the following parameters: VGS=3.9V, Vtn=1V, W/L=100, $\mu nCox=90\mu A/V^2$. Find I_D and $R_{DS.}$ [7M]

UNIT-II

3. a) Explain the problem of driving large capacitive loads? How such loads can be driven? [7M]
   b) Discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [7M]

(OR)

4. a) Explain about static, dynamic and domino logics with examples. [7M]
   b) How does depletion regions around source and drain are affected due to scaling down of device dimensions? Explain [7M]

UNIT-III

5. a) Draw the circuit diagram of single stage amplifier with resistive load and explain its operation. [7M]
   b) Explain the importance of body bias effect of a MOSFET in detail. [7M]

(OR)

6. a) Draw the circuit diagram of Common Drain amplifier and explain its operation. [7M]
   b) Write short notes on Modeling of transistor in detail. [7M]

UNIT-IV

7. a) Explain the operation of multiplexer based latches in detail. [7M]
   b) Write short notes on Meta stability in CMOS Logic. [7M]

(OR)

8. a) Draw the circuit diagram of SR Master Slave register and explain its operation. [7M]
   b) Write short notes on Ultra Deep-Submicron Era in detail. [7M]

UNIT-V

9. a) Write about FPGA Programming Technologies in detail. [7M]
   b) Explain the step by step approach of FPGA design process on Xilinx environment. [7M]

(OR)

10. a) Draw and explain the routing architecture of field programmable gate arrays. [7M]
    b) Write about the shift register design and implementation onto FPGA. [7M]

Code No: R2032042 **R20** SET -2

III B. Tech II Semester Regular Examinations, July -2023
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1.	a)	Give the steps for single metal CMOS n-well process and additional steps for bipolar devices.	[7M]
	b)	Explain how the Bi-CMOS inverter performance can be improved.	[7M]
		(OR)	
2.	a)	Determine pull-up to pull-down ratio of an NMOS inverter when driven through one or more pass transistors.	[7M]
	b)	Design a stick diagram for CMOS logic $Y= (A+B+C)^{/}$.	[7M]

UNIT-II

3.	a)	Discuss about NMOS transistor as a switch and PMOS transistor as a switch.	[7M]
	b)	Discuss the inverter delay and propagation delay.	[7M]
		(OR)	
4.	a)	Define scaling factor? Explain different types of device parameters.	[7M]
	b)	Two NMOS inverters are cascaded to drive a capacitive load CL=16Cg. Calculate pair delay Vin to Vout in terms of τ	[7M]

UNIT-III

5.	a)	Draw the circuit diagram of Common Gate amplifier and explain its operation.	[7M]
	b)	Explain the operation of MOSFET along with characteristics.	[7M]
		(OR)	
6.	a)	Explain the operation of single stage amplifier with diode connected load along with diagram.	[7M]
	b)	Write short notes on Modeling of transistor in detail.	[7M]

UNIT-IV

7.	a)	Explain the operation of Master-Slave Based Edge Triggered Register along with diagram.	[7M]
	b)	Write short notes on Cascading Dynamic Gates in detail.	[7M]
		(OR)	
8.	a)	Draw and explain the operation of Clocked CMOS register in detail.	[7M]
	b)	Write short notes on Complementary CMOS Logic in detail.	[7M]

UNIT-V

9.	a)	Write about Programmable I/O blocks in FPGAs.	[7M]
	b)	Explain about different programmable elements in FPGA architectures.	[7M]
		(OR)	
10.	a)	Explain the concept of Short channel effects in detail.	[7M]
	b)	Write the steps involved to prototype the HDL code onto FPGA device.	[7M]

Code No: R2032042 **R20** SET -3

III B. Tech II Semester Regular Examinations, July -2023
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1.	a)	Explain the steps in twin-tub process of CMOS fabrication with suitable sketch.	[7M]
	b)	What are the advantages of BICMOS process over CMOS technology?	[7M]
		(OR)	
2.	a)	Explain 2 µm Double Metal, Double Poly CMOS / Bi-CMOS Rules.	[7M]
	b)	Draw the circuit for NMOS inverter and explain its operation and characteristics.	[7M]

UNIT-II

3.	a)	What is meant by sheet resistance Rs? Explain the concept of Rs applied to MOS transistors.	[7M]
	b)	Calculate on resistance of an inverter from VDD to GND. If n- channel sheet resistance $R_{sn}=10^4\Omega$ per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4$ Ω per square.(Zpu=4:4 and Zpd=2:2)	[7M]
		(OR)	
4.	a)	What are the alternate gate circuits are available? Explain any one of item with suitable sketch.	[7M]
	b)	Write about the scaling limitations due to sub Supply voltages in MOSFETS.	[7M]

UNIT-III

5.	a)	List out different biasing styles of MOSFET and explain.	[7M]
	b)	List out advantages of Common Source amplifier in detail.	[7M]
		(OR)	
6.	a)	Explain the operation of Common Gate amplifier along with diagram.	[7M]
	b)	What is the term current sources and sinks and explain.	[7M]

UNIT-IV

7.	a)	What are the Issues in Dynamic Design and explain.	[7M]
	b)	Draw the circuit diagram of Clocked CMOS register and explain.	[7M]
		(OR)	
8.	a)	Draw the circuit diagram of Cross coupled NAND gates and explain .	[7M]
	b)	Explain the term setup time and hold time.	[7M]

UNIT-V

9.	a)	What is the need of a FPGA? And write its applications.	[7M]
	b)	Explain the basic architecture of FPGA along with diagram.	[7M]
		(OR)	
10.	a)	Write about FPGA families of different vendors.	[7M]
	b)	Write short notes on Metal Gate Technology in detail .	[7M]

Code No: R2032042 **R20** SET -4

III B. Tech II Semester Regular Examinations, July -2023
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1.	a)	What are the steps involved in the nMOS fabrication? Explain with neat sketches.	[7M]
	b)	List out few Comparison between CMOS and Bi-CMOS technology in detail.	[7M]
		(OR)	
2.	a)	Explain and derive the expressions for MOS transistor parameters gm, gds and ω0.	[7M]
	b)	Distinguish between nMos,pMos and CMOS fabrication process.	[7M]

UNIT-II

3.	a)	What are the limits on logic levels and supply voltage due to noise in scaling?	[7M]
	b)	What is inverter delay? How delay is calculated to for multiple stages?	[7M]
		(OR)	
4.	a)	Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.	[7M]
	b)	Explain scaling of MOS circuits. Give merits and demerits of scaling.	[7M]

UNIT-III

5.	a)	Draw and explain the operation of Common Source amplifier.	[7M]
	b)	Draw the circuit diagram of single stage amplifier with resistive load and explain its operation.	[7M]
		(OR)	
6.		Explain the following terms in detail (a) body bias effect (b) biasing styles	[14M]

UNIT-IV

7.	a)	Draw the circuit diagram of SR Master Slave register and explain its operation.	[7M]
	b)	Write short notes on pipelining.	[7M]
		(OR)	
8.	a)	Explain the importance of Pass-Transistor Logic along with example.	[7M]
	b)	How to find the Power Dissipation of Dynamic Logic and explain.	[7M]

UNIT-V

9.	a)	Explain the FPGA design flow in detail.	[7M]
	b)	Compare Full-Custom design with semi-custom design.	[7M]
		(OR)	
10.		Explain the following terms in detail (a) Fin-FET (b)TFET	[14M]