Code No: R2032042 **R20** SET -1

III B. Tech II Semester Regular/Supplementary Examinations, May/June -2024
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics. [7M]
   b) For a CMOS inverter calculates the shift in transfer characteristic curve when β_n/β_p ratio is varied from 1/1 to 10/1. [7M]

(OR)

2. a) Derive the equations for I_{ds} of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region? [7M]
   b) Draw the circuit for nMOS inverter and explain the transfer characteristic using necessary equations, and the different regions in the characteristics. [7M]

UNIT-II

3. a) List out the scaling factors for the different device parameters in terms of different scaling models? [7M]
   b) Calculate the ON resistance from V_{DD} to GND for the nMOS and CMOS inverter circuits. [7M]

(OR)

4. a) Explain the model for derivation of time delay? [7M]
   b) Discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [7M]

UNIT-III

5. a) Draw and explain the circuit diagram for common source amplifier and also construct input-output characteristics for the same? [7M]
   b) How do we maximize the voltage gain of a common-source stage? Explain [7M]

(OR)

6. a) Draw the small-signal equivalent circuit of diode connected MOSFET and measure the equivalent resistance? [7M]
   b) Calculate the output resistance of a simple current mirror. [7M]

UNIT-IV

7. a) Explain the different approaches used to reduce delays in large fan-in circuits? [7M]
   b) Draw the basic structure of a dynamic CMOS gate and explain the same? [7M]

(OR)

8. a) Explain about pass transistor logic. [7M]
   b) Draw and explain about SR Master slave register. [7M]

UNIT-V

9. a) Write down the step by step approach of FPGA design process on XILINX environment? [7M]
   b) Draw and explain the basic architecture of FPGA? [7M]

(OR)

10. a) Write about Drain Induced Barrier Lowering effect in nMOS transistor? Explain with neat sketch. [7M]
    b) List out the advantages and disadvantages of metal gate technology? [7M]

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Code No: R2032042 **R20** SET -2

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VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

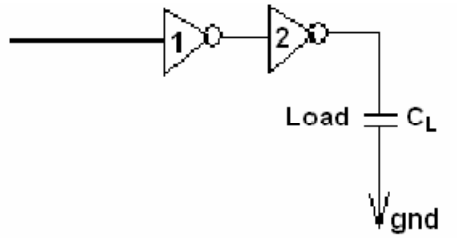
1. a) Explain in detail the p-well process for CMOS fabrication indicating the masks used. [7M]
   b) Tabulate the comparisons between n-well and p-well CMOS fabrication processes? [7M]

(OR)

2. a) What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter? [7M]
   b) Explain the different types of design rules and give some examples. [7M]

UNIT-II

3. a) What is sheet resistance? Derive the Expression for R_S? [7M]
   b) Two nMOS inverters are cascaded to drive a capacitive load C_L = 16 Cg. Calculate the pair delay in turns of τ for the inverter indicated in the figure below. What are the ratios of each inverter? [7M]



Inverter 1	Inverter 2
L_{PU} = 16 λ	L_{PU} = 2 λ
W_{PU} = 2 λ	W_{PU} = 2 λ
L_{Pd} = 2 λ	L_{Pd} = 2 λ
W_{Pd} = 2 λ	W_{Pd} = 8 λ

(OR)

4. a) What is the problem of driving large capacitive loads? Explain a method to drive such load. [7M]
   b) Briefly discuss about the scaling limits on logic levels and supply voltage due to noise? [7M]

UNIT-III

5. a) Draw the small-signal model for the MOS transistor. Briefly explain each component in that? [7M]
   b) Choose values of V_{GS} = 1,2,3,4 and 5V, assume that the channel modulation parameter is zero. Sketch to scale the output characteristics of an enhancement n-channel device if V_T = 0.7V and I_D = 500μA when V_{GS} = 5 V_{in} saturation. [7M]

(OR)

6. a) Derive the voltage gain equation for common source amplifier at high frequencies. [7M]
   b) Write short notes on current sinks and sources? [7M]

|'''|'|'|''||'''||||

UNIT-IV

7. a) Draw the basic one-transistor storage cell with cross-coupled latch sense amplifier and explain the operation with suitable timing diagrams? [7M]
   b) With EX-OR gate as an example explain about static and dynamic logics. [7M]

(OR)

8. a) Implement 4-input NAND gate using CPL and also construct the layout diagram for the same? [7M]
   b) With suitable diagrams explain how switch logic can be implemented using Pass Transistors and transmission gates? [7M]

UNIT-V

9. a) Give the steps in FPGA design flow with flow diagram and briefly discuss about each step. [7M]
   b) List out the various FPGA Boards and software tools required for digital system design? [7M]

(OR)

10. a) How does surface scattering affect the mobility of electrons in MOSFET? Explain with neat diagram. [7M]
    b) What is tunneling field effect transistor (TFET)? What are the advantages of using a TFET transistor? [7M]

Code No: R2032042 **R20** SET -3

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Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Explain the steps in twin-tub process of CMOS fabrication with suitable sketch. [7M]
   b) Tabulate the encoding scheme for a simple single metal nMOS process with respect to various MOS layers. [7M]

(OR)

2. a) Give the design rules for the following cases with neat sketches [7M]
   i) Polysilicon – polysilicon ii) n-type diffusion – n-type diffusion
   iii) n-type diffusion – p-type diffusion iv) metal 1 – metal 2.
   b) Show that the switching speed of an enhancement MOSFET varies inversely as the square of the channel length? [7M]

UNIT-II

3. a) What is inverter delay? How delay is calculated for multiple stages. [7M]
   b) How does depletion regions around source and drain are affected due to scaling down of device dimensions? Explain [7M]

(OR)

4. a) Explain about the constraints in choice of layers. [7M]
   b) Derive the expression for propagation delay in the case of cascaded pass transistors? [7M]

UNIT-III

5. a) With the help of neat circuit diagrams explain about CS stage with source degeneration? [7M]
   b) Derive an expression for transconductance and small-signal voltage gain for degenerated CS stage with the help of small-signal equivalent circuit? [7M]

(OR)

6. a) What is the need of source follower? Draw and explain the input-output characteristics of source follower? [7M]
   b) List out the comparisons between CS, CG and CD amplifier stages? [7M]

UNIT-IV

7. a) In gate logic compare the geometry aspects between two input nMOS NAND gate and CMOS NAND gate? [7M]
   b) Draw the positive latch using transmission gates and explain the operation? [7M]

(OR)

8. a) Explain about Domino CMOS logic. Draw the Domino structure for AND and OR gates? [7M]
   b) Draw the schematic circuit of a SR flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation? [7M]

UNIT-V

9. a) What are FPGAs? Explain about the principle and operation of FPGAs. What are its applications? [7M]
   b) List out the important features of Altera Flex 8000FPGA? [7M]

(OR)

10. a) With the help of neat diagram explain about impact ionization? [7M]
    b) What is giga-scale integration (GSI)? How does the gate delay scale down with improvement of semiconductor technology? [7M]

Code No: R2032042 **R20** SET -4

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VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1.	a)	With neat circuit diagram and transfer characteristics explain the operation of CMOS inverter?	[7M]
	b)	Draw the schematic, layout and stick diagram for two input nMOS NAND gates?	[7M]
		(OR)	
2.	a)	Discuss the alternative forms of pull-up for an inverter circuit. Compare the relative merits of three different forms of pull-ups?	[7M]
	b)	Draw the nMOS inverter circuit and determine the pull-up to pull-down ratio of an nMOS inverter driven by another nMOS inverter?	[7M]

UNIT-II

3.	a)	Why scaling is required? Write the scaling factors for different types of device parameters?	[7M]
	b)	Write notes on sheet resistance concept and its applications.	[7M]
		(OR)	
4.	a)	Explain the issues involved in driving large capacitor loads in VLSI circuit regions?	[7M]
	b)	Derive the expressions for rise time and fall time in the case of CMOS inverter.	[7M]

UNIT-III

5.	a)	Explain the small signal model for common source stage and sketch the drain current and trans conductance of transistor as a function of the input voltage?	[7M]
	b)	Explain briefly about body bias effect with neat diagrams?	[7M]
		(OR)	
6.	a)	Briefly discuss about CS stage with diode connected load and also draw the input-output characteristics?	[7M]
	b)	List out the applications of CS, CG and CD amplifier stages?	[7M]

UNIT-IV

7.	a)	What is level restoration? Explain the level restoring circuit with the help of neat sketch?	[7M]
	b)	What are the advantages and disadvantages of dynamic logic? Explain.	[7M]
		(OR)	
8.	a)	Draw the Master-slave positive edge-triggered register using multiplexers and explain the operation?	[7M]
	b)	What is pipelining? Explain the operation of two-phase pipelined circuit using dynamic registers?	[7M]

UNIT-V

9.	a)	Explain the following terms: i) LUT ii) CLB iii) IOB iv) Switch matrix	[7M]
	b)	List out the different FPGA families. Explain how they are differing.	[7M]
		(OR)	
10.	a)	Briefly discuss about velocity saturation effects in a Short Channel Si-MOSFET?	[7M]
	b)	What is a FinFET? What are the differences between FinFET and a multi-gate transistor?	[7M]